What is claimed is:

1. A semiconductor device,

wherein a plurality of TEGs comprising rectangular first electrode pads having a side length of 0.5 μm or shorter and constituted of an uppermost layer wiring are arranged in a scribe region.

2. A semiconductor device,

wherein a plurality of TEGs comprising rectangular first electrode pads having a side length of 1 μm or shorter and constituted of an uppermost layer wiring are arranged in a scribe region.

3. A semiconductor device,

wherein a plurality of TEGs comprising rectangular first electrode pads having a side length of 10 μm or shorter and constituted of an uppermost layer wiring are arranged in a scribe region.

4. A semiconductor device,

wherein a plurality of TEGs are arranged in a scribe region, said plurality of ETGs comprising rectangular first electrode pads having a side length of 10 μm or shorter and constituted of an uppermost layer wiring; and rectangular second electrode pads having a side length of 20 μm or longer and constituted of said uppermost layer wiring.

5. The semiconductor device according to claim 3,

wherein a plurality of TEGs comprising rectangular second electrode pads having a side length of 20 μm or longer and constituted of said uppermost layer wiring are further arranged in the scribe region.

6. The semiconductor device according to claim 3,

wherein a length of one side of said first electrode pad is not longer than the dimension obtained by adding a diameter of a connection hole between said first electrode pad and a lower layer wiring thereof and the length of an alignment margin between said first electrode pad and said connection hole.

7. The semiconductor device according to claim 3,

wherein a length of one side of said first electrode pad is about four-thirds of a diameter of a connection hole between said first electrode pad and a lower layer wiring thereof.

8. The semiconductor device according to claim 3,

wherein said scribe region is covered with a protection film.

9. The semiconductor device according to claim 3,

wherein said first electrode pad is exposed in an island shape.

10. The semiconductor device according to claim 5,

wherein a surface of said first electrode pad is covered with a protection film and a surface of said second electrode pad is partially exposed by removing said protection film.

11. The semiconductor device according to claim 4,

wherein said second electrode pad is connected commonly to a plurality of the TEGs.

12. The semiconductor device according to claim 5,

wherein said second electrode pad is connected commonly

to a plurality of the TEGs.

13. A semiconductor device,

wherein a plurality of TEGs comprising an extraction electrode constituted of an uppermost layer wiring are arranged in a product circuit region.

14. A method of measuring a semiconductor device,

wherein a plurality of TEGs comprising rectangular first electrode pads having a side length of 10 μm or shorter and constituted of an uppermost layer wiring, are arranged in a first scribe region while a surface of said first electrode pad is covered with a protection film, and

after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

15. The method of measuring a semiconductor device according to claim 14,

wherein an improvement of a yield of the semiconductor device is achieved.

16. The method of measuring a semiconductor device according to claim 14,

wherein said protection film on said first electrode pad is removed by a focused ion beam method or a selective etching method.

17. The method of measuring a semiconductor device according to claim 14,

wherein a plurality of TEGs comprising rectangular

second electrode pads having a side length of 20 μm or longer and constituted of said uppermost layer wiring, are further arranged in a second scribe region while a surface of said second electrode pad is partially exposed by removing said protection film on said second electrode pad.

18. A method of measuring a semiconductor device,

wherein a logic circuit is arranged in a product circuit region whose uppermost layer is covered with a protection film, and

after exposing a part of a surface of an extraction electrode constituted of an uppermost layer wiring by removing a predetermined part of said protection film, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said extraction electrode to evaluate a logic value of said logic circuit.

19. The method of measuring a semiconductor device according to claim 18,

wherein an improvement of a yield of the semiconductor device is achieved.

20. The method of measuring a semiconductor device according to claim 18,

wherein the predetermined part of said protection film is removed by a focused ion beam method or a selective etching method.

21. The method of measuring a semiconductor device according to claim 18,

wherein said logic circuit comprises n input terminals and m output terminals, and n + m + 3 probes are contacted to

said extraction electrodes to evaluate a logic value of said logic circuit.

22. The method of measuring a semiconductor device according to claim 21,

wherein one of said probes is a probe for contact confirmation.

23. A method of measuring a semiconductor device,

wherein a TEG is arranged in a product circuit region whose uppermost layer is covered with a protection film, and

after exposing a part of a surface of an extraction electrode constituted of an uppermost layer wiring by removing a predetermined part of said protection film, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said extraction electrode to evaluate said TEG.

24. The method of measuring a semiconductor device according to claim 23,

wherein an improvement of a yield of the semiconductor device is achieved.

25. The method of measuring a semiconductor device according to claim 23,

wherein a predetermined part of said protection film is removed by a focused ion beam method or a selective etching method.

26. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads in a scribe region, said pads having a side length of 10 μm or shorter and constituted of an uppermost layer wiring and forming a bonding

pad constituted of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and the patterning by the lithography method.

27. The method of manufacturing a semiconductor device according to claim 26,

wherein said step (a) includes the step of forming second electrode pads having a side length of 20 μm or longer and constituted of said uppermost layer wiring in said scribe region, and said step (c) includes the step of partially exposing a surface of said second electrode pad.

28. A method of manufacturing a semiconductor device, comprising the steps of:

(a) sequentially forming a first insulating film, a stopper insulating film, and a second insulating film on a semiconductor substrate;

(b) forming a connection hole in said first insulating film and forming a wiring trench in said stopper insulating film and said second insulating film;

(c) burying a conductor film in said connection hole and said wiring trench, and removing said conductor film in a region outside said connection hole and said wiring trench by a CMP method, thereby forming in a first scribe region a first

electrode pad formed together with a connection member;

(d) forming a protection film on an upper layer of said first electrode pad; and

(e) removing said protection film and said second insulating film in said first scribe region with said stopper insulating film used as an etching stopper layer, thereby exposing said first electrode pad.

29. The method of manufacturing a semiconductor device according to claim 28,

wherein said step (c) includes the step of forming in a product circuit region a bonding pad formed together with a connection member, said step (d) includes the step of forming a protection film on an upper layer of said bonding pad, and said step (e) includes the step of partially exposing a surface of said bonding pad by removing a predetermined part of said protection film in said product circuit region.

30. The method of manufacturing a semiconductor device according to claim 28,

wherein said step (c) includes the step of forming in a second scribe region a second electrode pad formed together with a connection member, and forming in a product circuit region a bonding pad formed together with a connection member, said step (d) includes the step of forming a protection film on an upper layer of said second electrode pad and said bonding pad, and said step (e) includes the step of removing a predetermined part of said protection film in said second scribe region, thereby partially exposing a surface of said second electrode pad, and removing a predetermined part of

said protection film in said product circuit region, thereby partially exposing a surface of said bonding pad.